AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6. (cancelled)

7. (currently amended) A semiconductor integrated circuit device including a reference voltage generating circuit, the reference voltage generating circuit comprising:~~according to claim 5,~~

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistive element which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistive element which is provided between the emitter of the second transistor and a first external terminal which supplies a ground potential of the circuit;

a third resistive element which is provided between a collector of the first transistor and a second external terminal which supplies a power source voltage;

a fourth resistive element which is provided between a collector of the second transistor and the second external terminal; and

a differential amplifier circuit having a CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, and which supplies the output voltage to bases of the first transistor and the second transistor in common,

wherein the first transistor and the second transistor are constituted by using a semiconductor region formed in a CMOS process associated with the differential amplifier circuit,

wherein the semiconductor integrated circuit device ~~which~~ includes a CMOS circuit having a second conductive-type well region and a first conductive-type well region formed on a first conductive-type semiconductor substrate, a first conductive-type MOSFET formed on the second conductive-type well region, and a second conductive-type MOSFET formed on the first conductive-type well region,

wherein the second conductive-type well region electrically separates the first conductive-type well region on which the second conductive-type MOSFET is formed from the first conductive-type semiconductor substrate, and

wherein each of the first transistor and the second transistor is formed of a bipolar transistor having a vertical structure with a second conductive-type diffusion layer, which is formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET, as an emitter portion, with a portion of a first conductive-type well arrangement, on which the second conductive-type diffusion layer constituting the emitter portion is formed, as a base portion, and with a portion of a second conductive-type well arrangement, which electrically separates said portion of the first conductive-type well arrangement from the first conductive-type semiconductor substrate, as a collector portion.

Claims 8-9. (cancelled)

10. (currently amended) A semiconductor integrated circuit device including a reference voltage generating circuit, the reference voltage generating circuit comprising:~~according to claim 9,~~

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistive element which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistive element which is provided between the emitter of the second transistor and a first external terminal which supplies a ground potential of the circuit;

a third resistive element which is provided between a collector of the first transistor and a second external terminal which supplies a power source voltage;

a fourth resistive element which is provided between a collector of the second transistor and the second external terminal; and

a differential amplifier circuit having a CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, and which supplies the output voltage to bases of the first transistor and the second transistor in common,

wherein the first transistor and the second transistor are constituted by using a semiconductor region formed in a CMOS process associated with the differential amplifier circuit,

wherein the semiconductor integrated circuit device includes a CMOS circuit having a second conductive-type well region and a first conductive-type well region formed on a first conductive-type semiconductor substrate, a first conductive-type MOSFET formed on the second conductive-type well region, and a second conductive-type MOSFET formed on the first conductive-type well region,

wherein each of the first transistor and the second transistor of the reference voltage generating circuit is formed of a bipolar transistor having a lateral structure with collector, emitter, and base portions being constituted by diffusion layers formed on respective portions of a first conductive-type well arrangement, the diffusion layers of the collector and emitter portions being formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET,

wherein the first conductive-type is a p-type and the second conducive-type is an n-type,

wherein the power source voltage supplied from the second external terminal is positive,

wherein the second transistor is constituted by one unit transistor, and

wherein the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.

11. (previously presented) A semiconductor integrated circuit device according to claim 10, wherein the first transistor is configured such that the plurality of unit transistors are formed on portions of the first conductive-type well arrangement having the same depth.

12. (previously presented) A semiconductor integrated circuit device according to claim 11, further comprising:

a power source circuit which generates an internal voltage, different from the power source voltage supplied from the second external terminal, based on a reference voltage from the reference voltage generating circuit;

an internal circuit which is operated by the power source circuit;

an input circuit which is operated based on the power source voltage supplied from the second external terminal to perform a level conversion of an input signal supplied from

a third external terminal and to transmit the converted input signal to the internal circuit; and

an output circuit which is operated based on the power source voltage supplied from the second external terminal to perform a level conversion of a signal generated by the internal circuit and to form an output signal to be outputted from the third external terminal,

wherein the differential amplifier circuit is constituted by a P-channel MOSFET and an N-channel MOSFET which are formed in the same process as MOSFETs which constitute the input circuit and the output circuit.

13. (previously presented) A semiconductor integrated circuit device according to claim 11, further comprising an internal circuit,

wherein an internal voltage is formed by reducing the power source voltage supplied from the second external terminal, and

the internal circuit is formed with a minimum forming size of a CMOS processing.

14. (previously presented) A semiconductor integrated circuit device according to claim 11, further comprising a power source circuit,

wherein the power source circuit includes a booster circuit and a negative voltage generating circuit which are operated at a constant voltage formed by using the reference voltage, and

voltages formed by the booster circuit and the negative voltage generating circuit are outputted as a gate drive voltage to drive a liquid crystal, a source drive voltage corresponding to image data, and a liquid crystal common electrode drive voltage.

15. (previously presented) A semiconductor integrated circuit device according to claim 7,

wherein the first conductive-type is a p-type and the second conducive-type is an n-type, and

wherein the power source voltage supplied from the second external terminal is positive.

Claim 16. (cancelled)

17. (previously presented) A semiconductor integrated circuit device according to claim 15,

wherein the second transistor is constituted by one unit transistor, and

wherein the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.

18. (currently amended) A semiconductor integrated circuit device including a reference voltage generating circuit, the reference voltage generating circuit comprising: ~~according to claim 16,~~

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistive element which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistive element which is provided between the emitter of the second transistor and a first external terminal which supplies a ground potential of the circuit;

a third resistive element which is provided between a collector of the first transistor and a second external terminal which supplies a power source voltage;

a fourth resistive element which is provided between a collector of the second transistor and the second external terminal; and

a differential amplifier circuit having a CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, and which supplies the output voltage to bases of the first transistor and the second transistor in common,

wherein the first transistor and the second transistor are constituted by using a semiconductor region formed in a CMOS process associated with the differential amplifier circuit,

wherein the semiconductor integrated circuit device includes a CMOS circuit having a second conductive-type well region and a first conductive-type well region formed on a second conductive-type semiconductor substrate, a first conductive-type MOSFET formed on the second conductive-type well region, and a second conductive-type MOSFET formed on the first conductive-type well region, and

wherein each of the first transistor and the second transistor of the reference voltage generating circuit is formed of a bipolar transistor having a lateral structure with collector, emitter, and base portions being constituted

by diffusion layers formed on respective portions of a first conductive-type well arrangement, the diffusion layers of the collector and emitter portions being formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET,

wherein the first conductive-type is a p-type and the second conducive-type is an n-type,

wherein the power source voltage supplied from the second external terminal is positive,

wherein the second transistor is constituted by one unit transistor, and

wherein the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.